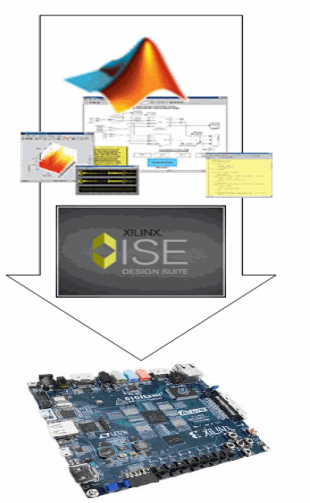
VIT
University
Vellore-632 014, Tamil Nadu, India.
www.vit.ac.in

Summer Training & Internship Program on

FPGA Applications using HDL Programming and Model based Design

2nd –14th June 2014



Organized by

TIFAC - CORE in AUTOMOTIVE INFOTRONICS

(Sponsored by Department of Science and Technology, Govt. of India)

Co - ordinators

Dr. K. Ganesan, Director, TIFAC CORE & Senior Professor, SITE

D. Muralidar, Assistant Professor, TIFAC CORE

D. Sridhar, Development Engineer, TIFAC CORE

TIFAC-CORE IN AUTOMOTIVE INFOTRONICS @VIT

- The centre is conducting need based training programs on cutting edge technologies for students, faculties and industry participants.
- Offering consultancy services for the industries and carrying out research works through the research grants received from funding agencies.
- The Centre has so far conducted 210 Training programs
- The centre has completed nearly 20 consultancy projects with many leading Automotive and Telecom companies.
- The centre has filed 16 patents.

Objective

- The purpose of the proposed program is to gain knowledge and hands-on experience in VLSI by HDL Programming and Model Based Programming .It focuses on Real Time Applications as well as to interface hardware with software to analyze them and to present them in an understandable manner.

- In this proposed program Hardware-in-Loop (HIL) based Implementation for FPGA solutions are going to be discussed. The reason for the use of a HIL process is becoming more prevalent in all industries is driven by two major factors: time to market and complexity.

- Today, Model Based Design has reached mainstream acceptance and is used in thousands of applications in industries from automotive to consumer electronics

General Requirements

- Students pursuing B. E / B. Tech / M. E / M.Tech degree / MS (SE) in any engineering discipline may apply for this Real Time Application Development using this Summer Internship Program. Applications will be reviewed and only 20 students will be selected by the coordinating committee of the program.

- During the first phase rigorous training will be given to students on both hardware and software modules. During the second phase (last few days) the participants will be given real time projects. During the third phase, the participants have to submit a project report and power point presentation, apart from (real time) project demo.

Topics to be covered:

1. Introduction to digital basics

- Combination Circuits
- Sequential Circuits

2. Structure of HDL module

- VHDL, Verilog

3. Operators - VHDL, Verilog

- Relational operators
- Arithmetic operators
- Shift and rotate operators

4. Data types

- VHDL data types
- Verilog data types

5. Data flow descriptions

- Signal declaration–VHDL, Verilog
- Assignment statements - VHDL, Verilog
- Concurrent signal assignment statements - VHDL, Verilog
- Delay time assignment -- VHDL, Verilog

6. Behavioral description

- Sequential statements - VHDL, Verilog
- If statements
- Signal and variable assignments
- Case statement
- Loop statement

7. Structural descriptions

- Named association -- VHDL, Verilog
- Positional association -- VHDL, Verilog

8. Common programming errors

- Structural modeling
- Data flow modeling
- Behavioral modeling

9. Procedure, tasks and functions in VHDL, Verilog

10. File processing in VHDL, Verilog

11. State machine modeling

- Moore state machine
- Mealy state machine

12. Synthesis

- Mapping signal assignment to gate level
- Mapping variable assignment to gate level synthesis mapping if, case and loop statements
- Mapping procedure, functions

13. Software

- Mentor graphics modelsim
- Xilinx ISE
- Digilent Adept

14. Hardware

- Atlys Spartan 6 development kit

15. Model Based Design for Image Processing Applications on FPGA

- Introduction to Digital Image Processing
- Image Enhancement Techniques
- Image Filtering
- Image Segmentation
- Introduction to Simulink and FPGA Design Flow
- Overview of Xilinx block sets and system modeling
- Model and simulate a DSP block using Simulink/ Xilinx System generator
- Concepts of Hardware co-simulation using System Generator DSP
- Algorithms Using Xilinx System Generator
- Processing Algorithms (Demo with Spartan 6)

Real Time project **Project report preparation** **PowerPoint presentation** **Project demonstration** — **to be done by students**

Targeted participants include:

- Students
- Research Scholars / Faculties
- Industry Participants

Course fees and duration

- Rs. 10,000/- (for Students)
- Rs. 20,000/- (for Faculties and Research Scholars)
- Rs. 30,000/- (for Industry Participants)
- **2 weeks from 2nd to 14th June 2014 (9.00 am to 6.00 pm)**
- Course material includes program contents in soft copy.
- Separate Training Certificate and Project Completion Certificate will be issued.

Payment through DD has drawn in favor of "TIFAC CORE, VIT University", Payable at Vellore.

Registration charges include Hand-outs, Lunch & Snacks. The number of participants is limited to **20**ased on first come first serve. Accommodation can be arranged in our Guest House on request based on first come first serve as per Tariff given below:

Tariff per day: Payment through cash (at guest house)

S. No.	Type Tariff	Rs.
1	Main Guest House A/C	2400.00
2	Guest House (Annexe) A/C	2000.00
3	Hostel Accommodation / Day / Head Without food*	300.00

***Separate DD to be sent for hostel accommodation charges (subjected to changes)**

Venue:

Room No.: 701, Technology Tower
7th Floor, VIT

Date / Time:

2nd–14th June 2014 **09.00 – 18.00 Hours**

Format for Registration confirmation

Summer Training & Internship Program on FPGA Applications using HDL Programming & Model based Design

2nd –14th June 2014

Name: ----------

Designation: ----------

Organization: ----------

Address: ----------

Phone: ----------Mobile----------

Fax: ----------E-mail: ----------

DD Details: ----------

Signature of the Participant

Please complete and mail or fax us above form **before 31st May 2014**

For Further Details Please Contact:

Registration :

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